Code No: R1931041 **R19** **SET - 1**

III B. Tech I Semester Regular Examinations, February-2022

LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) Explain the operation of an improved version of current mirror circuit with a neat circuit diagram. [8M]
   b) Design a regulated power supply using three-terminal IC to give V_o=+5 V, I_o=0.6 A, Vi=12 V_{DC}, T_A=60^{0}C. [7M]

(OR)

2. a) Explain the operation of dual input balanced output differential amplifier (ac equivalent) and derive the expressions for input resistance and output resistance. [8M]
   b) For an Op-amp, PSRR is 70 dB, CMRR is 10^5, and differential mode gain is 10^5. The output voltage changes by 20 V in 4 μs. Calculate: [7M]
      i) Common mode gain ii) Slew rate.

UNIT-II

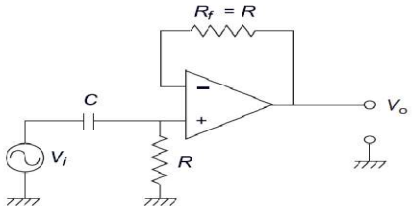
3. a) Draw the circuit diagram of a logarithmic amplifier using Op-Amps and explain its operation. [8M]
   b) Design an Op-amp based circuit to produce an output $-(V_1+2V_2-5V_3)$, where V_1, V_2 and V_3 are the input voltages. [7M]

(OR)

4. a) With a circuit diagram explain the working of a current to voltage converter. [8M]
   b) What are the differences between conventional rectifier and precision rectifier? Draw the circuit diagram of a full-wave precision rectifier using Op-amp. [7M]

UNIT-III

5. a) Consider the Op-amp high pass filter with 20 dB/decade roll-off shown below figure. Calculate the value of R if C = 0.001 μF and f_c = 15 kHz. [8M]

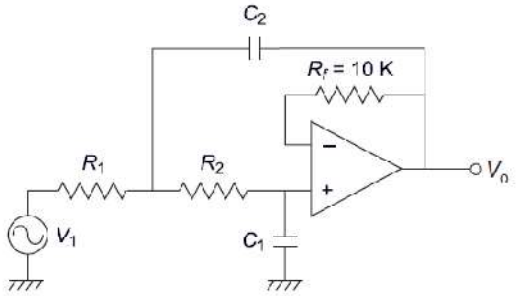


b) Draw the circuit for first-order lowpass filter and high pass filter and derive the expressions for cut-off frequencies. [7M]

(OR)

6. a) Give the design procedure for 60 dB/decade high pass filter in Butterworth configuration when the desired cut-off frequency is 200 Hz. [8M]

b) For the circuit shown, determine the values of R_1 and R_2 to get a cut-off frequency of 5 kHz. Assume C_1 = 0.01 μF. [7M]



UNIT-IV

7. a) Design a 555 astable multivibrator to operate at 10 kHz with 40% duty cycle. Assume necessary data. [8M]

b) Draw the circuit of a 565 PLL IC and explain its working. [7M]

(OR)

8. a) Design a square-wave generator using 555 timer for a frequency of 150 Hz and 70% duty cycle. Assume C = 0.1 mF. [8M]

b) How a phase locked loop is used as a FM demodulator? Explain with a neat diagram. [7M]

UNIT-V

9. a) Explain the counter type ADC with a neat block diagram and list out its disadvantages. [8M]

b) A 4-bit R-2R ladder type D/A converter having resistor values of R = 10 kΩ and 2R = 20 kΩ, uses V_R of 10V. [7M]
Find: i) the resolution of the D/A converter, and
ii) I_o for a digital input of 1101.

(OR)

10. a) Explain the working of dual slope-type of ADC with a neat diagram. [8M]

b) Explain the principle of inverted R-2R type DAC and write its advantages and disadvantages. [7M]

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