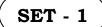
Code No: R193104B





III B. Tech I Semester Regular Examinations, February-2022 DIGITAL SYSTEM DESIGN USING HDL (Electronics and Communication Engineering)

Time: 3 hours

Max. Marks: 75

[8M]

Answer any **FIVE** Questions **ONE** Question from **Each unit** All Questions Carry Equal Marks

UNIT-I

- 1. a) Give the steps in FPGA design flow with flow diagram and briefly [8M] discuss about each step.
 - b) Explain about the principle and operation of FPGAs. What are its [7M] applications?

(OR)

- 2. a) Give the syntax of module representation in Verilog. Analyze the [8M] module structure in detail.
 - b) List out the various FPGA Boards and software tools required for [7M] digital system design.

<u>UNIT-II</u>

- 3. a) Explain the various data types supported by Verilog HDL. Give the [8M] necessary examples.
 - b) Analyze the FPGA implementation of addition operation with neat [7M] diagram.

(OR)

- 4. a) List out the different Operators available in Verilog HDL. Explain [8M] with example.
 - b) Explain about the predefined data values used for net or variable [7M] data type.

<u>UNIT-III</u>

- 5. a) Design a 4 bit full adder using gate level primitives.
 - b) Design a RS flip flop using NAND gates. Write a Verilog code for [7M] the same.

(OR)

- 6. a) Explain the design procedure for multiplexers and draw the logic [8M] diagram of a 4-to-1 line multiplexer with logic gates.
 - b) Implement the Verilog HDL module for a 4 to 1 vector multiplexer [7M] circuit using data flow level.

<u>UNIT-IV</u>

- 7. a) What is a frequency divider? Draw and explain the block diagram [8M] of a synchronous frequency divider?
 - b) Write a Verilog description of synchronous frequency divider. [7M]

Code No: R193104B



(OR)

- 8. a) Implement the digital clock application using asynchronous [8M] operations in Verilog.
 - b) Draw the circuit diagram of a 4-bit binary counter and explain its [7M] working with its function table.

UNIT-V

- 9. a) Explain the modeling approach for UART using Verilog HDL. [8M] Modeling approach consists of design and implementation?
 - b) Explain the sequence of operation for communicating with an I2C [7M] slave device?

(OR)

- 10. a) Explain the working principle of the PWM generator with neat [8M] diagrams.
 - b) Implement Verilog HDL source code for PWM generator. [7M]

2 of 2