Code No: R193104B **R19** **SET - 1**

III B. Tech I Semester Regular Examinations, February-2022

DIGITAL SYSTEM DESIGN USING HDL

(Electronics and Communication Engineering)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions **ONE** Question from **Each unit**
All Questions Carry Equal Marks
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UNIT-I

1. a) Give the steps in FPGA design flow with flow diagram and briefly discuss about each step. [8M]
   b) Explain about the principle and operation of FPGAs. What are its applications? [7M]

(OR)

2. a) Give the syntax of module representation in Verilog. Analyze the module structure in detail. [8M]
   b) List out the various FPGA Boards and software tools required for digital system design. [7M]

UNIT-II

3. a) Explain the various data types supported by Verilog HDL. Give the necessary examples. [8M]
   b) Analyze the FPGA implementation of addition operation with neat diagram. [7M]

(OR)

4. a) List out the different Operators available in Verilog HDL. Explain with example. [8M]
   b) Explain about the predefined data values used for net or variable data type. [7M]

UNIT-III

5. a) Design a 4 bit full adder using gate level primitives. [8M]
   b) Design a RS flip flop using NAND gates. Write a Verilog code for the same. [7M]

(OR)

6. a) Explain the design procedure for multiplexers and draw the logic diagram of a 4-to-1 line multiplexer with logic gates. [8M]
   b) Implement the Verilog HDL module for a 4 to 1 vector multiplexer circuit using data flow level. [7M]

UNIT-IV

7. a) What is a frequency divider? Draw and explain the block diagram of a synchronous frequency divider? [8M]
   b) Write a Verilog description of synchronous frequency divider. [7M]

(OR)

8. a) Implement the digital clock application using asynchronous operations in Verilog. [8M]
   b) Draw the circuit diagram of a 4-bit binary counter and explain its working with its function table. [7M]

UNIT-V

9. a) Explain the modeling approach for UART using Verilog HDL. Modeling approach consists of design and implementation? [8M]
   b) Explain the sequence of operation for communicating with an I2C slave device? [7M]

(OR)

10. a) Explain the working principle of the PWM generator with neat diagrams. [8M]
    b) Implement Verilog HDL source code for PWM generator. [7M]

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